Aim of the project: develop the building blocks for hybrid and monolithic pixel detectors for X-ray imaging at FELs and synchrotron light sources; build a demonstrator with a two-tier structure, including sensor and integrated front-end electronics in one layer and digital circuits in the other.

Involved INFN groups: Pavia, Pisa, Trento-TIFPA, Torino.

Proposed duration: 3 years.

Abstract

The use of large accelerator-driven X-ray sources, such as synchrotron light and free-electron lasers (FEL) facilities, continues to grow and expand to many scientific disciplines worldwide. A large number of synchrotron radiation sources is available around the world. Each of them features a large number of beam-lines, providing photons with wavelengths spanning from the atomic level to biological cells, which can be used as probes for advanced research in material science, physical and chemical science and in the medical and pharmaceutical fields. On the other hand, newly proposed X-ray FELs, with their outstanding properties in terms of brilliance and pulse duration, can offer unprecedented capabilities in penetrating the microscopic structure of organic and inorganic systems, new materials and matter under extreme conditions and in recording and understanding the time evolution of fast biochemical phenomena at the nanoscale. These facilities are now driving the state of the art of X-ray science, therefore shaping the requirements for many types of detectors. The XDET project aims to develop advanced instrumentation for X-ray imaging applications compliant with the very challenging specifications set by the FEL environment in terms of input dynamic range, processing speed, amplitude resolution and radiation hardness. The collaboration also plans to extend the use of the developed instrument to synchrotron light source experiments. The research will be pursued by following two different approaches, one based on hybrid, the other based on monolithic sensor technology.

The final deliverable for the monolithic sensor research line will consist of a detector prototype based on a two-tier structure and including a monolithic pixel sensor layer with integrated analog front-end and a digital layer incorporating high density memories and readout circuits. For the hybrid sensor research line, the collaboration will finally deliver the main building blocks for the construction of an X-ray camera based on hybrid technology. Vertical integration processes, in particular those enabling the fabrication of peripheral, low density through silicon vias (TSV), will also be explored by the collaboration in view of the design of a 2-tier, 4 side buttable detector tile.
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1 Introduction

In the next few years, X-ray free electron laser (FEL) facilities are expected to proliferate all around the world. Based on linear accelerator technology, X-ray FELs can provide coherent beams, femtosecond pulses and a brilliance ten orders of magnitude larger than storage ring based sources. With these features, they promise to revolutionize several research fields, including structural biology and chemistry, materials science and nuclear and molecular physics, or to start entirely new ones. New technologies currently under development, such as those based on energy recovery LINACs, inverse Compton scattering techniques and laser wake field accelerators, may lead to the design of even cheaper and more compact systems, further boosting the construction of new X-ray (or gamma-ray) sources. Machine upgrades are also planned or in progress in many synchrotron light source facilities, pushing the beam towards higher brilliance and shorter pulse duration. In this scenario, continuous improvement on the existing instrumentation for the different experimental needs, as well as training of skilled and qualified engineers and physicists, becomes of crucial importance to fully benefit of the outstanding properties of these powerful probing tools.

The XDET project aims at advancing the state of the art in the field of instrumentation for X-ray diffraction imaging at FELs and synchrotron light sources. For this purpose, the collaboration will work on the development of building blocks for advanced X-ray imagers following two different but synergetic research programs:

- one envisioning an approach based on **hybrid detector technologies**, where a pixel sensor with a high resistivity substrate is connected with a dual-layer front-end chip in a 65 nm CMOS technology, resulting in an overall three-layer structure;

- a second one pursuing a different line of action, based on **monolithic pixel technologies**, where the detector relies on a two-tier structure, with one layer consisting of a monolithic sensor with integrated front-end electronics and a second layer incorporating storage and digital readout.

The groups participating in the project have a strong background in the area of experimental particle physics and will take advantage of their experience in the field to propose innovative solutions and technologies in applications to photon science. Some of the groups were also part of the PixFEL experiment, funded by INFN in the last few years, whose purpose was to develop the main microelectronic building blocks and investigate the enabling technologies for the fabrication of high performance cameras in a hybrid technology for X-ray diffraction imaging at FELs. The XDET collaboration, in the first part of the research program, plans to characterize the final demonstrator of the PixFEL project, based on a 32×32, single-layer readout chip (PFM2, PixFEL front-end matrix 2) interconnected to a slim-edge pixel sensor, and a new version of the readout chip (PFM3, PixFEL front-end matrix 3), already submitted to an engineering run managed by CERN and suitable for post-processing with peripheral TSV technology. Both the demonstrator and the PFM3 chip are to be fabricated in 2017. Also by leveraging the outcomes of the PixFEL experiment and of the characterization of the PixFEL demonstrator and of the PFM3 chip, XDET aims at:

- bringing to a conclusion the activity carried out in the frame of the PixFEL collaboration by developing the digital readout layer of the two-tier front-end chip, in such a way to complete
the set of microelectronic building blocks needed to construct an X-ray camera based on hybrid pixel technology,

- building a demonstrator consisting of a 1 kpixel 2-tier detector for X-ray imaging with a monolithic sensor layer and a digital readout layer interconnected with a bump bonding technique.

Besides that, with respect to PixFEL, the XDET project will expand the collaboration to include solid-state physicists and chemists, part of the INFN Torino, INFN Pavia and TIFPA units, who, with their expertise as X-ray source users, will provide a tangible contribution to refining the characteristics and features of the devices under development and to their experimental validation.

2 Scientific and technical proposal

As already specified in the introduction, the research program of the XDET experiment intends to pursue two different approaches to the design of advanced pixel cameras for X-ray imaging at free electron lasers and synchrotron light sources. As a reference for the detector development, the collaboration will consider the requirements of X-ray diffraction imaging experiments at the European XFEL, under construction at DESY, Hamburg, currently representing the most challenging environment among the ones already operational or under construction.

The system will be designed with embedded programmable features making it suitable also for other experimental environments. In particular, besides considering other FEL facilities, the collaboration will explore the possibility to extend the use of the detectors to experiments at synchrotron radiation sources.

The reference specifications for the detector to be developed by the XDET experiment are listed in the following:

- 100 to 150 µm pitch;
- dead area ≤2%;
- ≥9 or 10 bit amplitude resolution, with in-pixel A/D conversion;
- ≥5 MHz conversion rate, with the capability to run at lower rates;
- conversion efficiency >90% for photon energies between 0.25 keV and 12 keV;
- input dynamic range covering at least 4 decades, from 1 to 10000 photons, in the different operating modes;
- resolution better than Poisson noise over the entire input range;
- for small signals (≤20 photons, where Poisson noise is less significant) single 1 keV photon resolution at 5 MHz conversion rate or larger, single 0.25 keV photon resolution at 1 MHz conversion rate or larger;
- capability to store at least 500 events (≥10 bits per event, 9 bit for amplitude measurement and at least 1 bit for error control) per pixel;
• capability to operate both in a direct readout mode (for FELs with constant pulse rate) and in a store-locally/read-out-later mode (for FELs operated in a burst mode, like in the case of the Eu-XFEL);

• for the part of the camera facing the diffracted X-ray beam, tolerance to several GGy of total ionizing dose; less severe requirements for the other layers in the structure, which are partially shielded by the first one.

The degree of compliance with the above specification list is expected to be different for the two approaches. For instance, it is anticipated that the detection efficiency of a 300 µm thick monolithic sensor for 10-keV X-rays is smaller than in the case of a 500 µm thick detector with a high resistivity substrate. Tolerance to ionizing radiation is another item where the two approaches may provide a fairly different response. In particular in the design of the detector based on the monolithic approach, specifications may be partially redefined according to the requirements for applications to synchrotron light source experiments and to the recommendations of X-ray source users, solid state physicists and chemists, who are part of the Pavia, TIFPA and Torino groups. Changes in the specifications might also be dictated by the characteristics of the technology chosen for the monolithic sensor layer. No such possibility exists for the case of the hybrid detector, whose main features have already been consolidated in the framework of the PixFEL project.

One goal of the program proposed by XDET is to improve on the performance of the X-ray cameras currently under development for the Eu-XFEL in terms of pixel pitch and, therefore, spatial resolution. This is accomplished in both the hybrid and monolithic sensor research line by adopting a more-than-Moore approach to the design of the front-end chip, i.e., by subdividing the pixel-level electronic blocks between two different layers, vertically interconnected with some integration technique. In this way, a larger functional density than in a standard mono-layer front-end chip fabricated in the same technology, or the same density as in a single-tier chip fabricated in a more scaled technology, can be achieved. Eventually, the solutions proposed by XDET will advance the state of the art of X-ray imagers by providing, in a single device, a combination of

• significantly smaller dead area (present proposed designs for the Eu-XFEL all exceed 10%),
• larger energy range for the incoming photons,
• larger in-pixel ADC resolution,
• larger on-board memory,
• flexibility in terms of readout modes.

The final deliverables of the XDET experiment will be

• for the hybrid detector research line, the set of microelectronic building blocks (the sensor in a high resistivity substrate and the two layers for the front-end chip) required for the construction of a hybrid detector-based X-ray imager,

• for the monolithic sensor research line, a 32×32 pixel demonstrator consisting of two layers interconnected with a bump bonding technique, with one layer including the collecting electrode together with the analog front-end electronics and the ADC and the other including the digital memory with fast readout electronics.

Some more details about the two research lines are provided in the following two sections.
2.1 Hybrid detector research line

The PixFEL experiment has developed a few building blocks for the construction of a three-tier X-ray camera based on a hybrid technology. In particular, the activity of the PixFEL collaboration led to the design and characterization of a front-end channel with dynamic compression, time variant shaping and in-pixel 10 bit analog to digital conversion in a 65 nm CMOS technology [1]. The collaboration also designed and tested fully depleted silicon detectors based on an active/slim edge process, which makes it possible to minimize the inactive area, and featuring a 500 µm thick substrate for improved detection efficiency at 12 keV photon energy [2]. As of July 2017, the fabrication of the PixFEL demonstrator, consisting of a slim edge pixel detector bump bonded to a readout chip called PFM2 (with 32×32 channels like the one described above), is in progress. In the same month, a new version of the readout chip, called PFM3 and designed to be compatible with a peripheral TSV process, has been submitted to the foundry for fabrication. One goal of the XDET project is to thoroughly characterize the PixFEL demonstrator and the PFM3 chip. The results from this activity, to be carried out mainly in the first year of the XDET project, will provide important information also for the design of the processing chain in the monolithic sensor research line.

The fully depleted pixel detector and the PFM2/PFM3 chips are actually 2 layers of a three-tier structure, which is shown in Fig. 1 and represents the long term goal of the PixFEL project. The third, bottom layer, part of a two-tier front-end chip (in yellow in the figure) including a processing chip like PFM2/PFM3 as its upper layer, is conceived to embed SRAM memories for data storage and digital readout circuits. It is worth emphasizing here that the PFM2 and PFM3 chips have been designed in such a way that they can be tested and read out, both standalone and connected.

Figure 1: conceptual view of a 3×3 detector matrix made of 9 four-side buttable elementary blocks.
to a pixel detector, without the third, digital layer. The digital readout chip will be developed in a 65 nm CMOS technology by the XDET collaboration. The production and test of the chip will complete the set of building blocks required for the construction of an X-ray camera based on the hybrid technology. Interconnection of the two layers of the front-end chip, requiring small size TSVs, is not part of the XDET research program. The chip will be designed in such a way that it can be used also as the second, digital layer for the detector based on a monolithic sensor technology. For this reason, some more details about it will be provided in the next section, concerning the monolithic detector research line. The collaboration will also explore peripheral TSV technologies, which are instrumental in the design of four-side buttable tiles for minimum dead area detectors. As this investigation is of interest for the second research line of the XDET program, peripheral TSV technologies will also be discussed in the next section.

One other goal of the XDET project is to complete the characterization of the edgeless sensors developed in the frame of the PixFEL project, in particular from the standpoint of the tolerance to doses in the range of tens of GGy. The microscopic damage of ionizing radiation in silicon oxides will also be investigated at a synchrotron light source under the supervision of the solid state physicists part of the TIFPA group.

### 2.2 Monolithic detector research line

Fig. 2 shows a conceptual view of the final demonstrator, with a detector based on monolithic CMOS technology to be delivered by XDET. This represents the main goal of the project. The

![Conceptual view of detector based on monolithic CMOS technology](image)

**Figure 2**: conceptual view of detector based on monolithic CMOS technology: one layer is devoted to sensor, analog front-end and ADC, the second one is used for data storing and readout.
device consists of two layers interconnected with a bump bonding technique. The first layer includes the collecting electrode, the analog front-end electronics and the in-pixel ADC. The second layer incorporates SRAM memories for frame storing and digital circuits for data readout. The two layers do not need to be fabricated in the same technology. Actually, in the case considered here, the bottom layer will be designed in a 65 nm CMOS process. For the upper layer, a process more suitable for monolithic sensor implementation will be used. More details about the key building blocks, technologies and design methodologies for the X-ray imager based on monolithic sensor technology are provided in the following.

2.2.1 Monolithic pixel sensors

The use of monolithic silicon pixel sensors, first introduced for imaging applications with visible light, has expanded in the last few years to charged particle tracking and X-ray detection. One very appealing characteristic of monolithic sensors is the potentially small size of the collecting electrode, resulting in a small capacitance and improved noise performance. One other advantage provided by monolithic pixels is the possibility to integrate the front-end electronics, or at least part of it, in the same substrate as the collecting electrode, therefore simplifying the detector structure. In the case of the detector proposed by XDET, this feature leads to reducing the number of layers to be interconnected from three in the hybrid approach to two in the monolithic approach, which means that high density TSVs are no longer needed to complete the vertically integrated structure. On the other hand, in general, monolithic sensors suffer from a poor detection efficiency, as far as X-rays are concerned, mainly due to the small depleted volume in the device substrate, limited to a few tens of microns at most. Some notable exceptions are represented by monolithic sensors in silicon on insulator (SOI) technology, where a high resistivity handle wafer can be used as the sensitive volume, and some recent development based on high voltage (HV) CMOS technologies. High resistivity substrate options are also available from a few foundries. However, also in these cases, full depletion of the substrate cannot be achieved, due to limitations on the maximum sensor bias voltage and to lack, in standard CMOS processes, of the needed processing steps.

In the monolithic detector research line, the XDET project intends to develop an X-ray imager based on a monolithic sensor with a fully depleted substrate. Promising candidate foundries are those providing access to high voltage technologies and/or high resistivity substrates, such as Towejazz, LFoundry, ESPROS and XFAB, to mention but a few. CMOS technology nodes between 130 nm and 180 nm will be considered. For the design of the sensing element, TCAD simulations will be extensively carried out to evaluate the impact of the different technological and geometrical options on device performance. The detection efficiency over a wide range of X-ray energies (0.25 keV - 10 keV) and the response times will be optimized. The so-called plasma effect, taking place in silicon sensors when a large amount of energy is released in a relatively small volume, will be investigated [3]. Guard ring design will be tuned to minimize performance degradation due to edge effects. The additional, post-processing steps, needed to accomplish full depletion of the substrate will be investigated. From this standpoint, contacts with the foundry technologists will be of paramount importance to share information about the adopted fabrication process.
2.2.2 Signal processing chain

One important goal of the XDET project, as far as this research line based on monolithic technology is concerned, is that of including in the monolithic sensor layer a large amount of functions, including charge signal amplification and shaping and analog to digital conversion. Fig. 3 shows a block diagram of the readout chain to be integrated with the collecting electrode. It includes a charge preamplifier, a time-variant trapezoidal shaper and a 10 bit ADC. More details about the design specifications can be found in the following.

Analog front-end. A 1 keV photon is converted to about 280 e-h pairs. Single 1 keV photon detection will therefore require an equivalent noise charge (ENC) $\leq 60$ electrons rms for the entire readout chain. For the detection of single 0.25 keV photons, an ENC $\leq 20$ electrons rms will be needed. This ensures an SNR$>3$ at the low end of the energy range. Note that power consumption is not a major concern here, as the final system will be relatively easy to access and cool down. Therefore, noise performance (and SNR) may be at least partly tuned by acting on the power dissipated in the very first stages of the chain. Covering the wide (1 to 10000 photons or more) input dynamic range while preserving single photon resolution at small signals is one of the most challenging tasks set by applications at FELs. The solution pursued in this research line of the XDET project will involve a charge preamplifier with a dynamically changing sensitivity based on the non linear feature of a MOS capacitor. This stage has been developed and successfully tested in the frame of the PixFEL project.

Signal shaping will be performed using a time variant technique, which, in the case of very short inter-bunch periods, like in the beam structure of the Eu-XFEL, can provide some advantage over continuous time processing in terms of time to return to baseline. Also, in particular when in-pixel analog-to-digital conversion is considered, a time variant shaper may be designed to provide the sample to convert directly at its own output.

In-pixel ADC. Analog data storage provides lower capacity than digital memories. Also, on-chip transmission of analog data, or transfer of analog samples from the pixel to the chip periphery
for digitization before data output, is more prone to corruption as compared to the case of in-pixel conversion. The downside of immediate digitization is the need for an ADC inside each pixel, with its clock running potentially close to other sensitive blocks. A SAR ADC can provide a good compromise between resolution and clock frequency. Another advantage of the SAR converter is that one new conversion bit becomes available at each clock cycle, and data transfer can start directly at the beginning of the sample conversion, without the need to wait for the end of the operation. A target sampling and conversion frequency of at least 5 MHz will be pursued in the design of the ADC, in such a way that the front-end chip is compliant with the experiments at the Eu-XFEL. A 9 bit resolution is the minimum required to get a quantization noise always smaller than Poisson noise in the case of a bi-linear characteristic, like the one to be implemented by the charge preamplifier.

**Calibration circuit.** The correct interpretation of the digital data sent off chip relies upon the accurate knowledge of the non linear input-output characteristics, or transcharacteristics, of the front-end channel. As the trans-characteristics may change from channel to channel due to process parameter dispersion, gain calibration has to be performed for each individual channel. This requires that a programmable signal generator circuit be integrated in each pixel. The granularity of the generated signal amplitude should be chosen to provide a significant number of experimental points in the input-output front-end curve and not to exceed the ADC resolution.

### 2.2.3 Memories and digital readout

The second layer of the detector will embed high density memory cells and digital readout circuits. A 65 nm CMOS process will be used for chip fabrication. One goal of XDET is to design the second layer in such a way that it can be used in both the hybrid and the monolithic sensor research lines.

**Digital layer design.** The elementary cell of the pixel detector, in its digital layer, will include a SRAM memory for data storage in applications with high event rates. A 65 nm CMOS technology should ensure enough room for at least 1 bit/µm². Each word will include 9 or 10 bits for amplitude measurement (depending on the ADC resolution) and at least 1 bit for error check. Based on the results from prototype characterization, including radiation tolerance tests, the need for more sophisticated error recognition methods will be evaluated. Memory address decoding will be defined based on power dissipation and circuit complexity considerations. The degree of parallelism in the data output will be established according to the number of available pads, the bandwidth requirements for the individual output channels and the resulting burden on the serializing circuits on the acquisition system. Particular attention will be devoted to the design of both the elementary memory cell (based on a 6T architecture) and the sensing circuits. Indeed, since the memory will be operated in harsh environment, accurate design will be required aiming at optimizing SRAM performance (e.g., limiting SEU induced bit-flip) and read-out reliability. In this frame, in a preliminary phase, storage capability could be traded-off with cell reliability (no. of transistors /cell vs. data stability), based on considerations coming from radiation hardening issues. Memory design will be carried out also as a step towards the development of a front-end chip based on vertical integration technologies, with one layer entirely devoted to data storage.
Design methodologies. As far as design methodologies are concerned, on the digital layer, the blocks will be mainly HDL-based (Verilog/VHDL) and modern Cadence digital tools will be used (RTL Compiler, Encounter Digital Implementation System) to perform logic synthesis and simulation, with STA/SSTA, SDC constraints, technology mapping and advanced synthesis options (low power, DFT and physical synthesis). The physical implementation of standard-cells will be done using automated place-and-route (PNR) tools: floorplanning, power planning, placement, clock tree synthesis (CTS), routing, DFM, optimization, design verification. A Digital on Top design will be used, with a top-down partitioning of the chip blocks, from the single pixel (or pixel region) to the End of Columns logic, including analog macro needed for example for biasing and monitoring and the necessary IP-blocks and the I/O stage. Timing and signal integrity will be checked using Cadence ETS/Tempus and taking into account the signoff power analysis (Cadence EPS/Voltus); the gate-level simulation with SDF back-annotation (Cadence Incisive environment) will be included also in the final chip verification. Additional Mixed-signal design and simulation (AMS environment) will be used at the sensitive interfaces between the analog circuitry and the digital.

Readout architecture. The choice of the readout architecture is mostly dependent on the beam structure of the specific FEL facility. FEL can be operated in continuous mode or in burst mode. Actually, only the Eu-XFEL will be made to work in a burst mode, where each burst includes 2700 photon pulses, with an inter-pulse period inside the burst of 220 ns. In the framework of the XDET project, the participating units intend to study the architecture for high-performance readout of a X-ray imager, to be implemented in the digital layer of the monolithic pixel based detector. The readout circuits will incorporate the needed degree of flexibility to switch between a continuous readout mode, which may be useful for applications at FELs and synchrotron light sources with low repetition rates (around 100 HZ), and a store & readout later mode, which is needed for fast event accumulation (suitable for operation at the Eu-XFEL).

2.2.4 Other ancillary blocks.

Other circuits may be needed to complete the set of fundamental building blocks. I/O circuits (transmitters and receivers, CMOS to LVDS and LVDS to CMOS converters) are needed to transfer data off-chip and to feed the clock to the ADC, the time variant shaper, the memory and the readout circuits. Power supply/temperature independent band-gap reference circuits are also required to provide stable voltage references to in-pixel blocks (e.g., the ADC). Other stages may be necessary to minimize the voltage drop across power and ground lines serving in-pixel circuits in a large matrix. Some of these circuits, especially those to be integrated in the digital layer in a 65 nm CMOS technology, may already be available as IP blocks from other INFN experiments currently in progress, like CHIPIX65 or CMS.

2.2.5 Interconnection and peripheral TSVs

Interconnection between the monolithic sensor layer and the digital layer, given the relatively large pitch of about 100 µm, can be easily achieved through bump-bonding techniques. A chip-to-chip bump bonding process is provided by the Fraunhofer Institute for Electronic Packaging and System Integration (IZM). A good yield was obtained with this technology by the ATLAS collaboration.
in the production of the pixel detector, featuring an effective bump bond pitch of 50 µm.

Use of low density, peripheral TSVs, which represent a key ingredient of a chip with minimum dead area, will be considered for both research lines in the XDET project. By accessing the input/output pads through the substrate, use of wire bonds can be avoided and integration with the system backend made easier. A low density TSV service is offered for instance by CEA-LETI and IZM in Europe and by Tohoku-MicroTec in Japan.

2.3 State of the art

Instruments for experiments at FELs and synchrotron light sources are, at present, in different stages of development. Their features are tailored to the specific beam line they will be working on. A short overview on the state of the art in the 2D X-ray instrumentation area is provided, limited to some significant examples selected among the large set of proposed solutions.

The European XFEL consortium is funding three independent detector developments, AGIPD, LPD and DSSC, all based on hybrid pixel technology. Each of them proposes a different solution to the challenges posed by the beam characteristics at the Eu-XFEL at DESY, in Hamburg, in particular the wide signal dynamic range (from 1 to 10000 photons) and the beam structure, where each pulse train includes about 3000 bunches at a 4.5 MHz rate [4].

AGIPD (Adaptive Gain Integrating Pixel Detector) [5] consists of a hybrid pixel array, with a readout ASIC (130 nm CMOS) bump-bonded to a silicon sensor. The front-end channel leverages a dynamic gain switching technique to cover the large input dynamic range, while an in-pixel analog pipeline is used to store the images recorded during each pulse train. 200 images per train can be recorded by the detector, corresponding to 200 storage capacitors integrated in a pixel area of 200 µm × 200 µm. The main scientific applications are coherent X-ray imaging and photon correlation spectroscopy at a 12 keV photon energy.

In the Large Pixel Detector (LPD) [4], the issue of large input dynamic range is addressed by using three different channels in parallel, each with a different gain setting and followed by its own analog pipeline. At 500 storage capacitors per pipeline, the cell pitch needs to be relatively large, 500 µm. The LPD front-end module will also include an interposer device in order to adapt the pitch difference between the silicon sensor and the ASIC. This solution also offers the advantage of adding an extra radiation shield, but may degrade the noise performance. The LPD focuses on the 12 keV photon energy range, optimally suited for the so-called liquid scattering experiments.

The DEPFET Sensor with Signal Compression (DSSC) [6] uses a nonlinear response in the sensing element of the pixel to cope with the large input dynamic range, and a digital memory for in-pixel data storage. Implementing the non linear response in the DEPFET sensor requires a complex fabrication process, resulting in long turnaround times. On the other hand, the very low noise performance of the DEPFET makes it an excellent candidate for the detection of low energy X-rays, ≤1 keV. The DSSC detector is made of hexagonal pixels with a 136 µm side, yielding a 200 µm bump-bond pitch. The front-end chip is designed in a 130 nm CMOS process and will include 64×64 elements. Data are digitized on-chip with an 8-bit single-slope ADC, whose operation is based on a 800 MHz clock driving a dual-edge counter. The memory consists of about 600 cells per pixel.

Three of the groups participating in the XDET project, namely the groups of Pavia, Pisa and TIFPA, are also part of the R&D PixFEL project, funded by INFN for the 2014-2016 period, which aims to develop the main microelectronic building blocks and to investigate the enabling...
technologies for X-ray diffraction imagers at FELs. The collaboration has already designed and successfully tested a prototype front-end channel, tailored for photon energies between 1 keV and 10 keV and including a charge preamplifier, a time variant shaper and a 10 bit ADC in a 110 μm pitch. A dynamic signal compression technique, based on the non linear feature of a MOS capacitor, has been adopted to comply with the large input dynamic range of 10000 photons. The detector is based on an active edge pixel sensor, guaranteeing about 2% dead area in a detector with an overall surface of 2.6 cm x 5.1 cm [1, 2].

The JUNGFRAU (adJUstiNg Gain detector FoR the Aramis User station) [7] pixel detector has been specifically developed for the Aramis beam line of the SwissFEL, under development at PSI. The system offers an input dynamic range of more than 10000 photons, managed with a signal compression technique very similar to the one adopted in the front-end chip of the AGIPD detector. The frame readout rate is about 2 kHz. The pixel pitch is 75 μm in both X and Y. The front-end chip has 4 analog outputs and analog to digital conversion is performed off-chip. A few CMOS MAPS based solutions have also been proposed, suitable for operation at much smaller rates than at the Eu-XFEL.

The Pixelated Energy Resolving CMOS Imager, Versatile and Large (Percival) [8] is based on a quadruple well 180 nm CMOS process and uses a 12 μm thick high resistivity epitaxial layer as the sensitive volume. This sets the maximum detectable photon energy to a few keV. On the other end of the spectrum, the good noise properties of the system make it possible to detect photons with energies of a few hundreds of eV. The project is pursuing the ambitious goal to fabricate a 25 μm pitch, 4k×4k pixel detector to be read out at a frame rate of 120 Hz or lower, suitable for operation at the LCLS (Linac Coherent Light Source) at Stanford.

The Silicon-On-Insulator PHoton Imaging Array Sensor (SOPHIAS) [9] is based on a CMOS silicon-on-insulator process targeting X-ray diffraction imaging experiments. The detector, featuring a 30 μm pitch, is designed to be sensitive to single photons in the 5.5- keV energy interval and to be operated at a frame readout rate of 60 Hz, suitable for operation at the SACLA source in Japan. Charge is processed using a typical CMOS MAPS scheme. The low degree of radiation hardness typical of this technology is mitigated by the shielding action of the 500 μm thick handle wafer also acting as the sensitive volume of the detector. The basic chip includes as many as 1.9 Mpixels.

Some developments in the field of monolithic detectors for charged particle tracking may actually be of interest also for the XDET research program. In particular, in the frame of the activities for ATLAS upgrade, high voltage CMOS technologies have been used to design monolithic pixel detectors with integrated charge preamplifier and comparator [10]. The elementary monolithic sensor cell also includes a D-to-A converter for fine tuning of the comparator threshold and electronic circuits providing pixel address information. The sensor is then read out by an FE-I4 chip.

Monolithic sensors, with full CMOS circuits directly built in the high-resistivity bulk silicon have also been developed and tested, in view of the design of rad-hard, highly efficient charged-particle and X-ray detectors [11]. The sensor relies on a double-sided processing, in particular on an N-type implantation on the backside for full substrate depletion and on a vertical junction termination structure for high-voltage isolation. As the P+/-type collecting electrodes are surrounded by an N-well, only PMOS transistors can be used for the front-end amplifier.
3 Description of the research activity

The proposed duration of the XDET project is 3 years.

3.1 Work packages

The activity of the XDET project will be subdivided into four work packages (WP) according to the following scheme:

WP1: Sensors design and testing (WP leader: Lucio Pancheri, University of Trento and TIFPA Trento). This WP will be concerned, mostly in the first year of the project, with the final characterization of the edgeless detector developed in the PixFEL project. In particular, the tolerance of the detector to doses well in excess of 1 GGy will be evaluated. Under the responsibility of the WP, a study of the microscopic damage of ionizing radiation in silicon oxides will also be performed at a synchrotron light source. For the monolithic sensor research line, in the frame of the WP1, extensive TCAD simulations will be carried out to evaluate the impact of the different technological and geometrical options on device performance and to optimize the detection efficiency and the time response. Post-processing steps required to accomplish full depletion of the sensor substrate will be investigated. Suitable test structures will be designed and produced to characterize the technology.

WP2: Analog front-end and ADC (WP leader: Massimo Manghisoni, University of Bergamo and INFN Pavia). This work package will be mainly addressing the design of the processing chain to be integrated in the monolithic sensor layer. The processing chain will include a charge preamplifier with dynamic signal compression, a time variant shaper and an ADC, according to the specifications discussed in the previous sections. In particular, the work package will concentrate on the development of the individual stages, to be included in a test chip, and on their integration in a 32×32 matrix to be interconnected to a digital storage and readout layer, as developed by the WP3.

WP3: Memories and digital readout (WP leader: Lino Demaria, INFN Torino). The activities of WP3 will focus on the design of memories for the storage of the digital data coming from the ADC developed in the frame of WP2. A 65 nm CMOS technology should ensure a storage density of more than 1 bit/µm². The word associated to each event (i.e., a single cell hit) will include 9/10 bits for amplitude measurement and at least 1 bit for error check. Based on the results from prototype characterization, including radiation tolerance tests, the need for more sophisticated error recognition methods will be evaluated. WP3 will also define the digital architecture and will implement a common environment for digital simulation and chip verification. Finally, the WP will be concerned with the IP blocks for data I/O, in particular digital drivers and receivers.

WP4: Prototype and demonstrator testing (WP leader: Fabio Morsani, INFN Pisa). This work package will take care of the test of the PFMS chip and of the PixFEL demonstrator, of the microelectronic chips developed in the XDET project and of the organization and execution of the test beam for the XDET demonstrator based on the monolithic sensor technology. The WP
activity will include the design and production of the test boards needed for the characterization of the various prototypes and demonstrators. It will also take care of the development of the DAQ boards for the test beam.

3.2 Workplan

The research activity of the XDET project will consist of the steps detailed in the following. For each task, the involved work packages are indicated.

2018

- Definition of the specifications for the design of advanced X-ray imagers at FELs (WP1, WP2, WP3);
- design of test structures with single blocks (charge preamplifier with signal compression, SAR ADC, circuits for gain calibration, single MOS capacitors); the structures will be integrated in a 1920 µm×1920 µm chip, available through Europractice with the mini@sic option, using a 65 nm CMOS technology (WP2);
- design of a 8×8 pixel matrix, with a 100 µm pitch with simple readout electronics (no data storage in-pixel); the matrix will be produced with the same mini@sic option as above (WP2);
- design of thick, standard pixel sensors (non active edge) in a high resistivity substrate (WP1);
- start of the investigation on readout electronics for advanced X-ray imagers at FELs (WP3, WP2).

2019

- Characterization of the pixel sensors developed in the first year, including the study of the ionizing radiation damage at high doses and of the plasma effect in high resistivity pixel sensors (WP1);
- design of thick, active edge pixel sensors and process tuning and optimization (WP1);
- begin the investigation on 3D integration processes, with particular emphasis on low density TSVs (WP1, WP2);
- characterization of the test structures in CMOS 65 nm technology produced during the first year runs (WP2, WP3);
- begin the investigation on the requirements for in-beam characterization of the device under development (WP3);
- start of the VHDL description of the readout electronics, based on the results from the investigation started in the first year of the project, and design of some elementary digital blocks (memory cells, buffers) (WP3);
• design of a readout chip featuring 32×32 channels with a 100 μm pitch; the design will take into account the requirements for low density TSVs fabrication; the readout architecture will not include in-pixel data storage; as an alternative option, to be decided based on the state of development of the readout architecture study, a few memory cells may be added to the pixel, in which case the pitch might increase and the number of cells in the matrix decrease; the 4.5 mm×4.5 mm chip will be designed in a 65 nm CMOS technology (WP2, WP3);

• design of the data acquisition system for the test beam (WP3).

2020

• Fabrication of low density TSVs in a few samples of the 32×32 matrix designed in the second year of the project (WP1);
• test of the 32×32 matrix designed during the second year of the project (WP2, WP3);
• test of the active edge pixel sensor;
• integration of the front-end chip with a pixel sensor (WP1);
• test of the chip after integration with the detector (WP1, WP2, WP3);
• begin the beam test organization (WP3);
• test structures with low density TSVs to assess the quality of the process (WP1, WP2, WP3);
• study of the ionizing radiation damage at high doses on the active edge pixel sensor designed in the second year of the project (WP1);
• production of the data acquisition system for the test beam (WP3);
• finalization of the VHDL description of the readout architecture (WP3);
• test of the chip interconnected with the pixel sensor in a beam (WP1, WP2, WP3).

Outlook for the activity following the PixFEL project. As already mentioned, the groups participating in the PixFEL project plan to complete the integration of the full system in the two/three years following the project conclusion. The final demonstrator of this five/six year research activity (including the three years of the PixFEL project) is expected to consist of a vertically integrated front-end chip with on board memory and fast readout architecture connected to an active edge sensor (as described in Section ??) together with a suitable data acquisition system. In order to complete the research program, the collaboration is committed to apply to national and European calls (including the calls issued in the framework of the Horizon 2020 program), also drawing on the outcomes of the activity carried out in the PixFEL project. Moreover, the proposing groups intend to expand the collaboration by including other teams with established expertise in the field of DAQ design. The group from INFN Bologna has already expressed its interest in participating in the final development and building of the 2D imaging system.
3.3 Description of the participating groups

3.3.1 University of Bergamo, University of Pavia and INFN Pavia

The research group at INFN Pavia has a wide experience in the field of the design of readout electronics for semiconductor detectors. The research interests are focused on low-noise, rad-hard preamplifiers as well as on mixed-signal (analog and digital) multichannel readout systems. The group is also involved in the study of nanoscale CMOS technologies and the characterization of devices in view of the implementation of low-noise, rad-hard front-end systems. These technologies are nowadays widely used for the development of readout integrated circuits for silicon strip and pixel detectors. The group is also working on the design of monolithic active pixel sensors (MAPS) with complete analog processing performed at the pixel level. Each element of the front-end section includes a classical binary readout circuit for capacitive detectors, with a charge preamplifier, a shaper and a threshold discriminator, and a set of digital blocks performing a pixel-level selective data readout (sparsification) and communicating with the digital readout section. The INFN Pavia unit is investigating new technology options to improve device features such as spatial resolution and charge collection efficiency. Vertical integration techniques have become very attractive for the design of advanced sensors and electronics since they provide a way to fabricate 3D multilayer structures including fully-depleted silicon detectors and mixed-signal readout circuits with high functional density. In the framework of the MAPS activity, the group is investigating the INMAPS quadruple well process, which employs, besides a deep n-well, a deep p-well placed underneath the n-well containing the p-channel devices thus preventing it from acting as a charge drain. Process features providing a higher resistivity epitaxial layer for faster and more efficient charge collection are also available in the same INMAPS technology. The high resistivity substrate improves the radiation tolerance to bulk damage. In the framework of the activity of the DSSC Consortium, an international collaboration aiming at the development of a mega-pixel camera for X-ray imaging at the European XFEL facility under construction in the Hamburg area (Germany), some members of the RU are involved in the design of basic building blocks for the DSSC chip. This chip is being developed for the readout of a novel non-linear DEPFET sensor with dynamic signal compression. For the research activity, the INFN Pavia group can take advantage of laboratories for the design and test of innovative devices and integrated circuits in semiconductor technologies. Using advanced software tools for device (Synopsys Sentaurus), circuit and system simulation (CADENCE Design System) and modern test instrumentation (Semiconductor Parameter Analyzer, Logic State Analyzer, Function/Arbitrary Waveform Generator, Network/Spectrum/Impedance Analyzer, Digital Oscilloscopes, Pulse/Pattern Generator) the group at INFN Pavia is able to design and characterize analog, digital and mixed-signal integrated circuits, single test devices and semiconductor sensors in nanoscale technologies.

3.3.2 University of Pisa and INFN Pisa

The Pisa group has been developing solid state radiation detector systems since the early 1980s, with important responsibilities in the design, construction and operation of the silicon systems for the experiments ALEPH (Vertex Detector) and BABAR (Silicon Vertex Tracker). More recently the activity has been focused on the development of fast pixel systems for low material charged particle trackers for future experiments at high intensity machines (Linear collider or Super B Factories). The activity has been funded through PRIN projects and through INFN experiments (SLIM5, ...
VIPIX, P-SuperB) and has been focused in two directions: CMOS-MAPS and hybrid pixels with high resistivity detectors. Prototypes with rate capability of 100 MHz/cm², 100 ns timestamp, and 50×50 µm² granularity have been realized with both triggered and datapush readout architectures with the ST 130 nm triple well process and with the INMAPS 180 nm quadruple well process. Vertical integration technologies with through-silicon-vias have also been employed to improve the performance of these devices. Micro channel cooling has also been developed to improve the heat removal process and reduce the amount of total material in the system. Within these R&D projects, the Pisa group has been involved in several activities:

- development of the in-pixel digital logic and of the readout architecture for large pixel matrices;
- optimization of the pixel sensor geometry;
- layout and simulation of the prototypes produced in different technologies (STM 130 nm, INMAPS 180 nm, Chartered/Tezzaron 130 nm);
- design and production of the testboard for the fabricated chips as well as the assembly of the prototypes;
- characterization of prototypes in laboratory, also with infrared laser and radioactive sources, and study of the performance of the devices with particle beams;
- study of radiation damage of the devices after irradiation with neutrons and photons from $^{60}\text{Co}$.

INFN Pisa has a very large controlled atmosphere laboratory with ISO7-ISO8 standard (class 10000 and 100000), for an area of 550 m² and 250 m², with all the equipment needed for the construction and testing of silicon detector systems: probe stations, electrical test equipment, wire-bonding stations, coordinate measurement machines, thermographic equipment, automated assembly station, a thermal chamber and thermo-fluidodynamics laboratory. Some of the available equipment is listed in the following:

- Manual Karl Suss Probe Station PM5, equipped with passive and active probes;
- HP4156B Semiconductor Parameter Analyzer;
- HP Spectrum Analyzer;
- Logic Analyzer and Pattern Generator Tektronix TLA715;
- Manual/semi/automatic deep access bonding machine: Kulicke & Soffa (K&S) 1470, K&S 8090, HUGES 470;
- Coordinate Measuring Machines (with and w/o probe contact): Mitutoyo F604, Mitutoyo BHN506;
- IR (1060 nm) laser and movable x-y table (25×25 cm²) for silicon detector characterization;
- Scopes: LeCroy waverunner 6050 4ch, BW 500 MHz - LeCroy SDA 740Zi 4ch, BW 4 GHz.
• WAVEFORM generators: Agilent 33220A 20 MHz function/arbitrary waveform generator, RIGOL DG5352 LXI 2-channel function/arbitrary waveform generator 350 MHz - 1 GS/s;

• X-ray tubes:
  – Microfocus tungsten anode source (Hamamatsu L9421-02) with focal spot size 5 µm (90 kV max, 200 µmA max);
  – Oxford Instruments Apogee X-ray tube with molybdenum anode, berillyum exit window, focal spot size 35 µm (50 kV max, 1 mA max).

3.3.3 University of Trento and INFN Trento (Gruppo Collegato)
The TREENTO Unit will conduct its activities in the Sensors & Micro Systems (SMS) Laboratory at the Department of Industrial Engineering of the University of Trento. The mission of the SMS laboratory, established in 2002, is the development, from the conceptual idea to the implementation of prototypes, of silicon based electronic sensors and MEMS (Micro Electro-Mechanical Systems). The expertise of the SMS group is mainly in the field of sensors and detectors for radiation imaging over a very broad energy range, including visible and ultraviolet light, X- and gamma-rays, and high-energy charged particles. The group has significantly contributed to the design of novel CMOS image sensors with special functionalities (e.g., high dynamic range, distance measurement features, multispectral capabilities, etc.) and is recognized as one of the leading groups in the development of silicon sensors for High Energy Physics applications. In the past few years, the research activity has been mainly oriented to silicon radiation detectors with three-dimensional electrodes and active edges, both within two INFN projects (National Scientific Committee V), TREDI (2005-2008) and TRIDEAS (2009-2012), and within the CERN ATLAS 3D Sensor Collaboration. The facilities available in the SMS Lab. include:

• workstations and software for the design and simulation of integrated circuits (Cadence IC package) and for the physical and technological modeling of the sensors (Synopsys TCAD);

• testing equipment for the electrical, electro-optical, and spectroscopic characterization of the circuits and sensors;

• thanks to the external support of Fondazione Bruno Kessler (FBK), further characterization tools are available; among them, a Scanning Electron Microscope (SEM) and Secondary Ion Mass Spectrometry (SIMS), and probe stations for electrical measurement at the die level.

3.4 Personnel involved in the project
Table 1 lists the personnel involved in the project, subdivided in the three participating groups, with the relevant commitment and coordination task. While Table 1 provides a fairly accurate indication of the people participating in the project, for the exact structure of the collaboration reference should be made to the PREVENTIVI 2014 INFN website. INFN Pisa has granted support to the project from the local mechanic workshop and electronics laboratory.
3.5 Financial plan

Tables from 2 to 4 provide the details of the three year financial plan for the three participating units. Table 5 provides a synoptic view of the global financial requests for the three years of the project. Table 2 to 5 provide the best estimate of the project budget. The financial requests are specified in their exact amount on the PREVENTIVI 2014 INFN website.
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<td>PhD Student</td>
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<tr>
<td>Francesco De Canio</td>
<td>Research Fellow</td>
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<td></td>
</tr>
<tr>
<td>Lorenzo Fabris</td>
<td>PhD Student and Senior R&amp;D Engineer, ORNL</td>
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<td></td>
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<tr>
<td>Marco Grassi</td>
<td>Research Fellow</td>
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<tr>
<td>Piero Malcovati</td>
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<tr>
<td>Massimo Manghisoni</td>
<td>Assistant Professor</td>
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<td>Local Coordinator and WP2 Leader</td>
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<td>Lodovico Ratti</td>
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<tr>
<td>Valerio Re</td>
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<td>Gianluca Traversi</td>
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<td>Stefano Bettarini</td>
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<td>Giulia Casarosa</td>
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<td>Francesco Forti</td>
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<td>Marcello Giorgi</td>
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<td>Fabio Morsani</td>
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<td>Eugenio Paolini</td>
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<td>Giuliana Rizzo</td>
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<td>Gian-Franco Dalla Betta</td>
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<td>Giorgio Fontana</td>
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<td>Hesong Xu</td>
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<td>Ekaterina Panina</td>
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<td>Giovanni Verzellesi</td>
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Table 1: personnel from the participating units.
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Table 2: financial plan for the Pavia unit (costs in kEuros).
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<td>Chip-to-sensor interconnection with IZM (2 wafers of sensors + 10 chips)</td>
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Table 3: financial plan for the Pisa unit (costs in kEuros).
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<td>production @ FBK</td>
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<td>(2,2 kEuro/lito eq.)</td>
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<td><strong>Total</strong></td>
<td>15,5</td>
<td>29,5</td>
<td>2,0</td>
</tr>
<tr>
<td>Investments</td>
<td>0,0</td>
<td>0,0</td>
<td>0,0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>18,0</td>
<td>34,0</td>
<td>11,0</td>
</tr>
</tbody>
</table>

Table 4: financial plan for the Trento unit (costs in kEuros).
### Travels

<table>
<thead>
<tr>
<th>Year</th>
<th>Pavia</th>
<th>Pisa</th>
<th>Trento</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>2014</td>
<td>11.0</td>
<td>8.0</td>
<td>2.5</td>
<td>21.5</td>
</tr>
<tr>
<td>2015</td>
<td>13.0</td>
<td>10.0</td>
<td>4.5</td>
<td>27.5</td>
</tr>
<tr>
<td>2015</td>
<td>9.0</td>
<td>16.0</td>
<td>9.0</td>
<td>34.0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>33.0</strong></td>
<td><strong>34.0</strong></td>
<td><strong>16.0</strong></td>
<td><strong>83.0</strong></td>
</tr>
</tbody>
</table>

### Consumables

<table>
<thead>
<tr>
<th>Year</th>
<th>Pavia</th>
<th>Pisa</th>
<th>Trento</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>2014</td>
<td>49.0</td>
<td>5.0</td>
<td>15.5</td>
<td>69.5</td>
</tr>
<tr>
<td>2015</td>
<td>89.0</td>
<td>56.0</td>
<td>29.5</td>
<td>174.5</td>
</tr>
<tr>
<td>2015</td>
<td>129.0</td>
<td>5.0</td>
<td>2.0</td>
<td>136.0</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>267.0</strong></td>
<td><strong>66.0</strong></td>
<td><strong>47.0</strong></td>
<td><strong>380.0</strong></td>
</tr>
</tbody>
</table>

| **Total** | **300.0** | **100.0** | **63.0** | **463.0** |

Table 5: global financial plan (costs in kEuros).

### 3.6 Milestones and deliverables

Milestones and deliverables proposed for the three years of the project are listed in the following. Of course, the milestones and deliverables for the second and third year of the project might change depending on the evolution of the research activity.

#### 3.6.1 Milestones

**2014**

1. The specifications for the design of an advanced, 2D X-ray imager are defined (30/06).
2. An analog channel with signal compression features is designed and submitted (31/12).
3. A 9-bit SAR ADC is designed and submitted (31/12).
4. A standard fully depleted pixel sensor is designed and submitted (31/12).

**2015**

1. The structures from the first year run are tested (30/06).
2. The standard pixel sensor designed in the first year is tested (30/06).
3. A thick, active edge fully depleted pixel detector is designed and submitted (31/10).
4. A 32×32 readout chip with a 100 µm pitch is designed and submitted (31/12).
1. The 32×32 readout chip is tested (30/06).
2. The active edge pixel sensor designed in the second year is tested (30/06).
3. The 32×32 readout chip is connected to a pixel sensor and the full detector is tested (31/12).
4. The VHDL description of the readout architecture is completed (31/12).

3.6.2 Deliverables

2014
- Detector specifications.

2015
- Wafer with standard fully depleted pixel sensors.
- Chips with single blocks and with an 8×8 matrix, in a 65 nm CMOS technology.

2016
- Wafer with active edge, fully depleted pixel sensors.
- 32×32 readout chip with 100 μm pitch.
- 32×32 readout chip interconnected with the sensor.
- 32×32 readout chip with low density interconnect.
- VHDL description of the readout architecture.

4 Significance of the project and expected scientific, technological and social impact

This project aims at laying the foundations for developing an X-ray imaging device for applications to experiments at free electron laser facilities, therefore providing the community of FEL users with a high performance instrument based on advanced solutions from the standpoint of both architecture and technology. The ultimate goal is to advance the state-of-the-art of microelectronic instrumentation for FEL experiments, in such a way that progress is facilitated in strategic fields of life science and material science and, ultimately, in key sectors like health care, green transportation and quality of life enhancement. Because of the aggressive specifications of the sensors developed, the knowledge gained through this project will also benefit other fields of radiation instrumentation, where fast, minimum dead area, intelligent pixel sensors are needed, such as particle trackers in high energy physics experiments, beam monitors for hadrontherapy, devices for medical radio-diagnostic systems. The program is expected to spawn significant advancements in microelectronic circuit
design for imaging sensors. This will be achieved also by means of the application of state-of-the-art interconnection processes and pixel sensor fabrication technologies to scientific instrumentation. The program of the PixFEL project is also fully compliant with the key objectives of the Horizon 2020 European Framework Program. It will support excellent science by training young researchers and involving them in cutting-edge technological and scientific R&D activities concerning radiation detection and microelectronics. The collaboration will be involved in the development of devices based on emerging microelectronic integration technologies. The activity carried out in the PixFEL project will also help improve the European research infrastructure by laying the foundations for the development of advanced instrumentation to be used for the broad science program envisioned at FELs. Finally, this activity will foster international collaborations between institutions involved in the design and/or use of FEL facilities.

5 Synergies with other INFN experiments and national and/or international projects

The research activity to be carried out in the PixFEL project, especially for what concerns the investigation of vertical integration technologies and the development of slim edge sensors and microelectronic circuits in 65 nm CMOS process may take advantage of the cooperation with other projects and experiments, some of which also funded by INFN, where some of the members of this collaboration are involved and will be involved in the coming years.

- In the framework of the Work Package 3 (Microelectronics and Interconnection Technologies), the AIDA project is exploring 3D technologies and developing building blocks for new readout chips in view of applications to radiation detection systems. In particular, the Task 3.1 of the work package (3D interconnection) aims at bringing together the community of physicists and engineers involved in the design and development of the next generation particle physics instrumentation and using the collective effort to build common demonstrators suitable for testing the different vertical integration solutions proposed by industry and research labs. Task 3.2 (Shareable IP Blocks for HEP) has the goal of designing and qualifying some individual microelectronic blocks (e.g., band-gap references, digital to analog and analog to digital converters, voltage regulators, I/O blocks) which can be included in more complex readout chips to be used in a vertically integrated configuration with a radiation detector. Most of the IP blocks under development in this task are based on a 65 nm CMOS technology.

- The CMS and ATLAS collaborations have proposed a new R&D project, pursuing the development of pixel readout integrated circuits. The collaboration is meant to address some major challenges posed on several fronts by the experiments at the High Luminosity (HL) LHC: smaller pixels to resolve tracks in boosted jets, very high hit rates, unprecedented radiation levels, very large output bandwidth, to mention some. In this activity, 65 nm CMOS has been identified as a particularly promising technology.

- CERN has recently finalized a market survey to get appropriate access to a 65 nm CMOS technology from TSMC foundry through IMEC. TSMC (Taiwan Semiconductor Manufacturing Company) is one of the largest IC foundries in the world. IMEC is a very well-known
European research institute, which provides support and services for the European IC University and small enterprise program (Europractice).

- The CMS collaboration, in which some of the members taking part in the PixFEL project are involved, is starting a research activity for the development of a momentum discriminating tracker for the CMS experiment at the HL-LHC. The design of the front-end chip will be based on the 65 nm CMOS technology adopted at CERN. The investigation of radiation hardness issues at very high integrated doses (of the order of 1 Grad), which is pursued by the collaboration in view of the luminosity upgrade of the LHC machine, is of relevance to the X-ray detector applications at FELs.

6 Risk assessment and mitigation strategies

Active edge sensors represent a relatively recent technology, finding itself at an early stage of development. While encouraging results have already been obtained in the test of the first prototypes, the fabrication steps, including trench etching, polysilicon trench filling and handle wafer removal still need some optimization. Production of the sensors for the PixFEL project also has to take into account the quantum efficiency requirements of experiments at FELs, setting a constraint on the detector thickness, which has to be no smaller than 450 µm, in order for the sensor to be capable of detecting photons in the 10 keV energy range. To mitigate the risk of failure in this part of the project and have a 100 µm pitch pixel sensor available for interconnection to the 32×32 readout chip, a standard fully depleted pixel sensor will be designed and fabricated during the early part of the project.

Characterization in a particle beam plays in general an important role in the qualification of a radiation detector. The groups participating in the PixFEL project (and in particular the Pisa group) have a longstanding experience in the organization of tests of radiation detectors for particle tracking in particle beams. With respect to the case of position sensitive detectors, characterization of X-ray imaging devices obviously requires a different kind of beam and a different acquisition system, which needs to be developed if it is not available at the test facilities. Therefore, the organization of a test beam in the time frame of the PixFEL experiment appears to be a critical task. However, characterization of the full detector, including the sensor interconnected to the 32×32 pixel readout chip, will be at least carried in laboratory with an infra-red laser source and with X-ray tubes, which are already available among the collaborating teams.

As already mentioned, low density TSVs represent a key step for the assembly of a large area X-ray imaging detector with minimum dead area. As this is an emerging, non fully established technology, a risk of partial or total failure in the manufacturing of the through silicon vias, involving substrate thinning and via etching and formation, has to be accounted for. As a mitigation strategy, in the design of the front-end, 32×32 chip and in the sensor to front-end chip assembly, the option for standard wire bonding from bond pads on the front of the chip to the test PCB will be retained.
References


